I claim:

1. A clock generation circuit for slewing a clock frequency from an initial clock frequency to a final clock frequency, the clock generation circuit comprising:

an oscillator comprising a plurality of phase outputs; and

a modulator coupled to the oscillator and adapted:

to set a current frequency divider value to an initial frequency divider value, the initial frequency divider value corresponding to the initial clock frequency;

to modify a period of a feedback signal through a plurality of periods from an initial period to a final period, the modify operation utilizing one or more of the plurality of phase outputs; and

to change the current frequency divider value when the period of the feedback signal reaches the final period;

wherein the modulator is adapted to perform the modify and change operations until the current frequency divider value reaches a final frequency divider value, the final frequency divider value corresponding to the final clock frequency.

2. The clock generation circuit of claim 1, wherein the clock generation circuit comprises a portion of an integrated circuit.

3. The clock generation circuit of claim 1, wherein:

the modify operation increases the period of the feedback signal relative to the initial period and the change operation increases the current frequency divider value.

4. The clock generation circuit of claim 1, wherein:

the modify operation decreases the period of the feedback signal relative to the initial period and the change operation decreases the current frequency divider value.

5. The clock generation circuit of claim 1, wherein the modulator is further adapted:

to modify the period of the feedback signal by selecting, for each of the plurality of periods through which the period was modified, one or more of the plurality of phase outputs and a corresponding frequency divider value for each of the one or more phase outputs, each corresponding frequency divider value used to modify the current frequency divider value.

6. The clock generation circuit of claim 1, wherein the modulator further produces first and second control signals and wherein the clock generation circuit further comprises:

a feedback divider and multiplexer circuit coupled to the plurality of phase outputs of the oscillator, adapted to receive the first and second control signals and producing the feedback signal, the feedback divider and multiplexer circuit adapted:

to couple, based on the first control signal, a selected phase output as the feedback signal; and

to divide a frequency of at least the selected phase output by a value equivalent to the current frequency divider value modified by a corresponding frequency divider value, the value corresponding to the second control signal.

7. The clock generation circuit of claim 1, wherein the oscillator comprises an input and the clock generation circuit further comprises:

a Phase Frequency Detector (PFD) comprising at least one PFD output, a first input adapted to receive the feedback signal, and a second input adapted to receive a reference clock signal; and

a charge pump and loop filter module having at least one input coupled to the at least one PFD output and an output coupled to the input of the oscillator.

8. The clock generation circuit of claim 1, wherein the modulator further comprises a memory comprising a plurality of entries, each entry comprising a phase value and a relative frequency divider memory value, wherein the modulator is further adapted, when performing each modify operation, to select one of the phase outputs by using a phase value from a given

entry in the memory and to select a corresponding relative frequency divider value from the relative frequency divider memory value in the given entry.

9. The clock generation circuit of claim 1, wherein modification of the period of the feedback signal creates a fractional frequency divider value, wherein the modulator further comprises a memory comprising a plurality of entries, each entry comprising a phase value, wherein each of the modify operations is performed at least in part by accessing entries in the memory, wherein a portion of the entries in the memory is adapted to create fractional frequency divider values that decrease as the entries are traversed from a starting entry to an ending entry.

10. The clock generation circuit of claim 9, wherein the clock generation circuit further comprises a down-to-up profile converter adapted to convert phase values in the entries in the portion of memory from phase values that decrease as the entries are traversed from the starting entry to the ending entry to phase values that increase as the entries are traversed from the starting entry to the ending entry, wherein the down-to-up converter is also adapted to determine frequency divider memory values corresponding to certain of the phase values to modify the period of the feedback signal, the convert and determine operations adapted to create fractional frequency divider values that increase as the entries are traversed from the starting entry to the ending entry.

11. The clock generation circuit of claim 1, wherein modification of the period of the feedback signal creates a fractional frequency divider value, wherein the modulator further comprises a memory comprising a plurality of entries, each entry comprising a phase value, wherein each of modify operations is performed at least in part by accessing entries in the memory, wherein a portion of the entries in the memory is adapted to create fractional frequency divider values that increase as the entries are traversed from a starting entry to an ending entry.

12. The clock generation circuit of claim 1, wherein the modulator further comprises a memory comprising a plurality of entries, wherein the modulator further comprises a start memory location register and an end location register and wherein the modulator is further

adapted, when performing the modify operations, to start at a start memory location from the start memory location register and end at an end memory location from the end memory location register.

13. The clock generation circuit of claim 12, wherein the modulator is further adapted to perform the change operation when the end memory location is reached.

14. The clock generation circuit of claim 1, wherein the modulator further produces first and second control signals and comprises a memory having at least one relative frequency divider value, the first control signal corresponds to one of the plurality of phase outputs, and the clock generation circuit further comprises:

a plurality of feedback dividers, each feedback divider coupled to an associated one of the phase outputs, adapted to receive the second control signal and adapted to divide frequency of the associated phase output by a value corresponding to the second control signal to create a divided phase output, the value determined utilizing the current frequency divider value and a given one of the at least one relative frequency divider values; and

a multiplexer coupled to each of the divided phase outputs, adapted to receive the first control signal and adapted to output, based on the first control signal, one of the divided phase outputs as the feedback signal.

15. The clock generation circuit of claim 1, wherein the modulator further produces first and second control signals and comprising a memory having at least one relative frequency divider value, the first control signal corresponds to one of the plurality of phase outputs, and the clock generation circuit further comprises:

a multiplexer coupled to each of the phase outputs, adapted to receive the first control signal and adapted to couple, based on the first control signal, one of the phase outputs to a feedback divider as a multiplexer output; and

the feedback divider coupled to the multiplexer output, adapted to receive the second control signal and adapted to divide frequency of the multiplexer output by a value corresponding to the second control signal to create the feedback signal, the value determined

from the current frequency divider value and a given one of the at least one relative frequency divider values.

16. The clock generation circuit of claim 1, wherein modification of the period of the feedback signal creates a fractional frequency divider value, wherein the modulator is further adapted to perform a first modify operation so that a first fractional frequency divider value is created and to perform a second modify operation so that a second fractional frequency divider value is created, and wherein the first and second fractional frequency divider values are different.

17. The clock generation circuit of claim 16, wherein the difference comprises a predetermined fractional difference.

18. The clock generation circuit of claim 1, wherein the modulator is further adapted to modify the period of the feedback signal by selecting, for each modify operation for a period, at least two given phase output of the plurality of phase outputs and at least one given corresponding relative frequency divider value, wherein the modulator is adapted to select one of the at least one given corresponding frequency divider values to be a function of the current frequency divider value when a selected given phase output of the at least two given phase outputs passes a phase change point relative to a previously selected given phase output of the at least two given phase outputs.

19. The clock generation circuit of claim 1, wherein the plurality of periods is of a number equivalent to or less than that of the plurality of phase outputs.

20. The clock generation circuit of claim 1, wherein the modulator is further adapted to perform the modify operation in order to spread clock frequency between a nominal clock frequency and a lower down-spread clock frequency.

21. The clock generation circuit of claim 1, wherein the modulator is further adapted to perform the modify operation in order to spread clock frequency between a low clock frequency and a high clock frequency, each of the low and high clock frequencies being approximately equidistant from a nominal clock frequency.

22. The clock generation circuit of claim 1, wherein each of the initial and final clock frequencies comprises a nominal clock frequency.

23. An integrated circuit comprising:

at least one clock generation circuit comprising:

an oscillator adapted to generate a plurality of phase outputs; and

a modulator coupled to the oscillator and adapted:

to set a current frequency divider value to an initial frequency divider value, the initial frequency divider value corresponding to an initial clock frequency;

to modify a period of a feedback signal through a plurality of periods from an initial period to a final period, the modify operation utilizing one or more of the plurality of phase outputs; and

to change the current frequency divider value when the period of the feedback signal reaches the final period;

wherein the modulator is adapted to perform the modify and change operations until the current frequency divider value reaches a final frequency divider value, the final frequency divider value corresponding to a final clock frequency.

24. The integrated circuit of claim 23, wherein the modulator further produces first and second control signals and comprises a memory having at least one relative frequency divider value, the first control signal corresponds to one of the plurality of phase outputs, and the clock generation circuit further comprises:

a plurality of feedback dividers, each feedback divider coupled to an associated one of the phase outputs, adapted to receive the second control signal and adapted to divide frequency of the associated phase output by a value corresponding to the second control signal to

create a divided phase output, the value determined utilizing the current frequency divider value and a given one of the at least one relative frequency divider values; and

a multiplexer coupled to each of the divided phase outputs, adapted to receive the first control signal and adapted to output, based on the first control signal, one of the divided phase outputs as the feedback signal.

25. The integrated circuit of claim 23, wherein modification of the period of the feedback signal creates a fractional frequency divider value, wherein the modulator is further adapted to perform a first modify operation so that a first fractional frequency divider value is created and to perform a second modify operation so that a second fractional frequency divider value is created, and wherein the first and second fractional frequency divider values are different.

26. The integrated circuit of claim 23, wherein each of the initial and final clock frequencies comprises a nominal clock frequency.

27. A method for slewing a clock frequency from an initial clock frequency to a final clock frequency, the method comprising the steps of:

providing a plurality of phase outputs of an oscillator;

setting a current frequency divider value to an initial frequency divider value, the initial frequency divider value corresponding to the initial clock frequency;

modifying a period of a feedback signal through a plurality of periods from an initial period to a final period, the modify operation utilizing one or more of the plurality of phase outputs; and

changing the current frequency divider value when the period of the feedback signal reaches the final period;

wherein the steps of modifying and changing are performed until the current frequency divider value reaches a final frequency divider value, the final frequency divider value corresponding to the final clock frequency.

28. An integrated circuit comprising:

an oscillator adapted to generate a plurality of phase outputs; and

a modulator coupled to the oscillator, comprising a memory having a plurality of first updated frequency divider values, and adapted:

to set a current frequency divider value to an initial frequency divider value, the initial frequency divider value corresponding to an initial clock frequency;

to modify a period of a feedback signal through a plurality of periods from an initial period to a final period, the modify operation utilizing one or more of the plurality of phase outputs and one or more of the first updated frequency divider values; and

to change the current frequency divider value when the period of the feedback signal reaches the final period, the change operation creating a second updated frequency divider value;

wherein the modulator is adapted to perform the modify and change operations until the current frequency divider value reaches a final frequency divider value, the final frequency divider value corresponding to a final clock frequency; and

one or more frequency dividers coupled to the modulator, each frequency divider adapted to divide one or more frequencies of one or more of the phase outputs by the first and second updated frequency divider values.

29. The integrated circuit of claim 28, wherein each of the initial and final clock frequencies comprises a nominal clock frequency.

30. The integrated circuit of claim 28, wherein the modulator is further adapted to perform the modify operation in order to spread clock frequency between a nominal clock frequency and one or more spread clock frequencies.

31. The integrated circuit of claim 30, wherein the wherein the modulator is further adapted to perform the change operation in order to spread clock frequency between the nominal clock frequency and the one or more spread clock frequencies.